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VadaTech Announces a XMC with Xilinx Kintex Ultrascale + FPGA, onboard PLL and front optical option

Henderson, NV – November 15, 2023 – VadaTech, a leading manufacturer of integrated systems, embedded boards, enabling software and application-ready platforms, announces the XMC500. The XMC500 is an XMC module per VITA 42 specification and based on the Xilinx Kintex Ultrascale+ FPGA XCKU11P. The XMC500 interfaces to the host via x8 PCIe Gen3 (other protocols such as 1G/10G/40G, Aurora, SRIO, etc. are possible by programming the FPGA) and also has dual bank of DDR-4 memory (32-bit wide) for a total of 8GB of memory.

The module follows the VITA 46.9 and routes I/O to XMC P16 as X24s+X8d+X12d. Two of the X24s are used for the 1PPS and sine wave input as sync clock to the on board PLL. There are six LVDS input/output (could be configured in any combination as single ended +1.8V) and ten GPIO +3.3V. Ten of the X12d are high speed SERDES that connect directly to the MGT Bank of the FPGA.

The 10 high speed SERDES going to the P16 could be configured for PCIe or non-PCIe protocols. There are two hard core PCIe and some of the valid PCIe configuration are show below:

- No PCIe
- x8 PCIe and x2 PCIe
- x4 PCIe, x4 not PCIe and x2
- PCIe x8 not PCIe and x2 PCIe

There are many other combinatorial to take advance of smaller PCIe lanes to add more lanes to the non-PCIe protocols such as:

- x1 PCIe, x7 not PCIe, x1 PCIe and x1 not PCIe

The module has an option for the front panel Optical via MTP/MPO optics which can operate up to 25G per lane. This allows operations such as 100Gb ethernet. Since the FPGA is programable any protocol could be run on these lanes with mix and match including PCIe, Aurora, etc.

The XMC500 has an on board PLL which can generate any frequency to the MGT banks. The PLL can lock into a 1PPS or 10Mhz (or any sine wave input up to 300MHz) clock. The sync clocks have their input thru the front panel or thru the P16 connectors. User can select the sync input and the priority. The XMC500 could still operate and generate any clock to the MGT without any sync reference clock. The PLL on the board has hitless fail over its input sync clocks. The PLL has an OCXO for stability reference and XO as the jitter reference.

The module is available in both air cooled and conduction cooled versions. Please consult with VadaTech Sales to discuss products and specific ordering options.

About VadaTech

VadaTech provides innovative embedded computing solutions from board-level products, chassis-level platforms, to configurable application-ready systems. With a focus on AdvancedTCA, MicroTCA, VPX and PCIe solutions, the company offers unmatched product selection and expertise. A unique combination of electrical, mechanical, software, and system-level expertise, enables VadaTech to provide customized commercial or rugged computing solutions to meet the most complex customer requirements. VadaTech also offers specialized product solutions for VME, CompactPCI, and other architectures. A member of PICMG and VITA, VadaTech has headquarters, design and manufacturing facilities in Henderson, NV with design, support and sales offices in Europe and Asia Pacific.

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